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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/633,004
Filing Date: July 31, 2003
Appellant(s): SINGH ET AL.

Kevin J. Zilka
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 09/05/06 appealing from the Office action mailed 03/17/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,707,156	SUZUKI ET AL.	3-2004
6,100,589	TANAKA	8-2000

Applicants' Admitted Prior Art of Figures 1-2.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 2, 4-18, 20, 21, 27, 29 and 30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not disclose an entirety of at least one of the transistors is disposed directly below the bond pad, as recited in claim 1, 20 and 21.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4 – 18, 20, 27, 29 and 30, insofar as in compliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (PN 6,707,156) in view of Tanaka (PN 6,100,589).

Suzuki et al. discloses, as shown in Figure 1, an integrated circuit, comprising:

an active circuit (13);

a metal layer (M1L-M10L) disposed, at least partially, above the active circuit;

a bond pad (M11L) disposed, at least partially, above the metal layer;

wherein the metal layer is disposed, at least partially, directly above the active circuit;

wherein the metal layer ensures that bonds are capable of being placed over the active circuit and/or the at least one transistor;

wherein the active circuit includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad.

Suzuki et al. does not disclose the metal layer defines a mesh. However, Tanaka discloses an integrated circuit comprising a metal layer (200, 300) defined a mesh. Note Figures 1-22 of Tanaka. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit of Suzuki et al. having the metal layer defined a mesh, such as taught by Tanaka in order to further improve the mechanical strength and to

further enhance the effects for suppressing crack formation in the insulation interlayer so that it inherently prevents the damage to the active circuit and/or the at least one transistor during the bonding process.

Regarding claim 4, Suzuki et al. and Tanaka disclose the metal layer includes an interconnect metal layer.

Regarding claim 5, Suzuki et al. and Tanaka disclose the interconnect metal layer interconnects the bond pad with a plurality of underlying metal layers.

Regarding claim 6, Suzuki et al. and Tanaka disclose each of the underlying metal layers is in electrical communication by way of a plurality of vias (110a-c, 120a-c, 123a-b, 124a-b, 125a-b, 612a-b, 614a-b, 616a-b, 618a-b).

Regarding claim 7, Suzuki et al. and Tanaka disclose the metal layer includes a plurality of openings (130a-i, 133a-i).

Regarding claim 8, it is inherent that the openings of Suzuki et al. and Tanaka are adapted for facilitating an interlock between the metal layer and an inter-metal dielectric layer disposed between the metal layer and the bond pad.

Regarding claim 9, Suzuki et al. and Tanaka disclose the inter-metal dielectric layer is constructed from a material selected from the group consisting of a low-K dielectric material [Col. 6, lines 35-44].

Regarding claim 10, Suzuki et al. and Tanaka disclose the openings are completely enclosed around a periphery thereof [Figures 2A, 6A, 7A, 9A of Tanaka].

Regarding claim 11, Suzuki et al. and Tanaka disclose the openings have a substantially square configuration [Figures 2A, 6A, 7A, 9A of Tanaka].

Regarding claim 12, Suzuki et al. and Tanaka disclose the openings define a plurality of substantially linear first portions and a plurality of substantially linear second portions which intersect [Figures 2A, 6A, 7A, 9A of Tanaka].

Regarding claim 13, Suzuki et al. and Tanaka disclose the openings define a matrix of openings.

Regarding claim 14, Suzuki et al. and Tanaka disclose a plurality of interconnect vias are formed in rows along the first portions [Figures 2A, 6A, 7A, 9A of Tanaka].

Regarding claim 15, Suzuki et al. and Tanaka disclose the interconnect vias are spaced along a length of the first portions [Figures 2A, 6A, 7A, 9A of Tanaka].

Regarding claim 16, Suzuki et al. and Tanaka disclose the interconnect vias include one single row for each of the first portions [Figures 2A, 6A, 7A, 9A of Tanaka].

Regarding claim 17, Suzuki et al. and Tanaka disclose the interconnect vias include at least two spaced rows for each of the first portions [Figure 9A of Tanaka].

Regarding claim 18, Suzuki et al. and Tanaka disclose a width of the fist portions is enlarged to accommodate the at least two spaced rows for each of the first portions [Figure 9A of Tanaka].

Regarding claim 20, Suzuki et al. discloses, as shown in Figure 1, an integrated circuit, comprising:

an active circuit means (13) for processing electrical signals;

a metal layer (M1L-M10L) disposed, at least partially, above the active circuit means and including a metal layer means for preventing damage incurred during a bonding process;

a bond pad (M11L) disposed, at least partially, above the metal layer;

wherein the metal layer is disposed, at least partially, directly above the active circuit means;

wherein the metal layer ensures that bonds are capable of being placed over the active circuit means and/or the at least one transistor;

wherein the active circuit means includes a plurality of transistors, and an entirety of at least one of the transistors (13) is disposed directly below the bond pad.

Suzuki et al. does not disclose the metal layer defines a mesh. However, Tanaka discloses an integrated circuit comprising a metal layer (200, 300) defined a mesh. Note Figures 1-22 of Tanaka. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit of Suzuki et al. having the metal layer defined a mesh, such as taught by Tanaka in order to further improve the mechanical strength and to further enhance the effects for suppressing crack formation in the insulation interlayer so that it inherently prevents the damage to the active circuit and/or the at least one transistor during the bonding process.

Regarding claim 27, Suzuki et al. and Tanaka disclose the metal layer is disposed, at least partially, above the active circuit along a vertical axis.

Regarding claim 29, Suzuki et al. and Tanaka disclose the inter-metal dielectric layer is constructed from a low-K dielectric material (polyimide and FSG). Note Figure 1, Col. 1, lines 39-51 and Col. 7, lines 26-38 of Suzuki et al..

Regarding claim 30, Suzuki et al. and Tanaka disclose the inter-metal dielectric layer is fluorinated silica glass (FSG) material. Note Figure 1, Col. 1, lines 39-51 and Col. 7, lines 26-38 of Suzuki et al..

3. Claims 2 and 21, in so far as in compliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (PN 6,707,156, of record) in view of Tanaka (PN 6,100,589, of record) and further in view of Applicants' Admitted Prior Art of Figures 1-2.

Suzuki et al. and Tanaka disclose the claimed invention including the integrated circuit as explained in the rejection above. Suzuki et al. and Tanaka does not disclose the active circuit including an input/output bus and a plurality of vertically spaced underlying metal layers, at least partially, under the active circuit. However, Applicants' Admitted Prior Art of Figures 1-2 disclose an active circuit (102,104) including an input/output bus (104) and a plurality of vertically spaced underlying metal layers (M1-M4), at least partially, under the active circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Suzuki et al. and Tanaka having the active circuit including an input/output bus and a plurality of vertically spaced underlying metal layers, at least partially, under the active circuit, such as taught by Applicants' Admitted Prior Art of Figures 1-2 in order to provide the interconnects between the device and the external connection, and to integrate the multi-layer interconnect structures to perform a plurality of functions.

(10) Response to Argument

Appellant argued that the claims clearly meet the written description requirement. This argument is not convincing for the following reasons: Yet, it is disclosed that the active circuit may include a plurality of transistors. Yet it is disclosed a plurality of transistors forming a core of circuits. Yet it is disclosed the bond pads 306 may be disposed above the core 302, and/or any

other part of the active circuit 308. However, there is nothing in the instant application discloses an entirety of at least one of the transistors being disposed directly below the bond pad. Note that the bond pad 306 may be disposed above the core and/or any other part of the active circuit and the active circuit may include a plurality of transistors, but it does not necessarily mean an entirety of at least one of the transistors being disposed directly below the bond pad. Also note that it was the typo in the final rejection about the claimed numbers. The claims should be 1, 2, 4-18, 20, 21, 27, 29 and 30.

Appellant argued that Tanaka simply does not address the problem of bonding-related damage to the active circuit and that Suzuki does not even mention bonding. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In fact, Suzuki discloses, as shown in Figure 1 and Col. 4, lines 58-64, that layer M11L is used as the pad, and an entirety of at least one of the transistors 13 is disposed directly below the pad. It is certainly that the pad is used as a connection to a wire or a bump. Suzuki further discloses that the stress is occurred between the wiring layers and the crack could be formed in the insulating layers between the wiring layers.

On the other hand, Tanaka discloses, as shown in Figures 1, 2A, 2B, 6A – 9B, 19-22, and Col. 7, line 47 – Col. 8, line 48, the meshed metal layer 200 that has the openings 130a – 130i, and props composed of insulating interlayer are provided between the metal layers. Tanaka

further discloses that, by forming the meshed metal layer, no cracks form in the insulating interlayer even if a load is applied during wire-bonding. Therefore, it would be obvious to combine the teaching of Tanaka into the Suzuki's invention to further improve the mechanical strength and to further enhance the effects for suppressing crack formation in the insulating interlayer so that it inherently prevents the damage to the active circuit and/or the at least one transistor.

Appellant argued that Tanaka does not disclose a width of the first portion is enlarged to accommodate the at least two spaced rows for each of the first portions, as recited in claim 18. This argument is not convincing because Tanaka discloses, as shown in Figures 9A and 9B, a width of the first portion is enlarged to accommodate the at least two spaced rows (612a, 614a, 122a) for each of the first portions.

Appellant argued, that the references when combined fail to teach or suggest all of the claim limitations, as recited in claim 2. This argument is not convincing because the combination of references of record discloses all of the claim limitations of claim 2, as explained in the rejection above.

Appellant argued that Tanaka does not disclose the interconnect vias include at least two spaced rows for each of the first portions, as recited in claim 17. This argument is not convincing because Tanaka discloses, as shown in Figures 9A and 9B, the interconnect vias include at least two spaced rows (612a, 614a, 122a) for each of the first portions.

Appellant argued that the references do not disclose meshed interconnect metal layer disposed, at least partially, above the I/O bus of the active circuit. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In fact, Suzuki discloses, as shown in Figure 1 and Col. 4, lines 58-64, that the integrated circuit comprising an active circuit (13), a metal layer (M1L-M10L) disposed, at least partially, above the active circuit, a pad (M11L), and an entirety of at least one of the transistors (13) is disposed directly below the pad. Suzuki does not disclose the metal layer is meshed.

Tanaka discloses, as shown in Figures 1, 2A, 2B, 6A – 9B, 19-22, and Col. 7, line 47 – Col. 8, line 48, the metal layer (200) is meshed.

Suzuki and Tanaka does not disclose the active circuit including an input/output (I/O) bus and a plurality of vertical spaced underlying metal layers disposed, at least partially, under the active circuit and around a periphery. However, Applicants' Admitted Prior Art of Figures 1 and 2, disclose the active circuit including an input/output (I/O) bus and a plurality of vertical spaced underlying metal layers disposed, at least partially, under the active circuit and around a periphery.

The combination of Suzuki, Tanaka and Applicants' Admitted Prior Art of Figures 1 and 2, teaches the meshed metal layer forms above the active circuit, wherein the active circuit

includes the input/output bus. Therefore, the meshed metal layer forms above the input/output bus.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Hung Vu

Conferees:

Richard T. Elms

Hung Vu

DOUGLAS W. OWENS
PRIMARY EXAMINER